REMARKS

Review and reconsideration on the merits are requested.

Claims 1-7 and 15-21 are active. They were rejected in the final rejection of December 12, 2005 as anticipated by U.S. Publication No. 2005/0145879 A1 Nakayama et al (Nakayama). Applicants amend the claims and traverse this rejection.

The amendment was discussed with the Examiner during a telephone interview on March 9, 2006. The Examiner was questioned as to whether the amendment would avoid the anticipation rejection over Nakayama and the Examiner indicated that he was not in a position to commit without considering the matter after the filing of a request for continued examination.

Traversal

Claim 1 is currently amended. It calls for:

1. (currently amended): A nitride semiconductor substrate having a diameter of 10 mm ~~or more, which has a single layer structure composed of~~ or more comprising a nitride semiconductor layer having a basic composition represented by $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$), ~~or a multi-layer structure comprising said nitride semiconductor layer,~~ the mass density of said nitride semiconductor layer being 98% or more of a theoretical mass density ρ (x) represented by the following general formula (1):

$$\rho(x) = \frac{4(M_x + M_N)}{\sqrt{3}a_x^2 c_x N_a} \cdots \quad (1)$$

,

wherein $a_x = a_{GaN} + (a_{AlN} - a_{GaN})x$, wherein a_{GaN} represents an a-axis length of GaN, and a_{AlN} represents an a-axis length of AlN; $c_x = c_{GaN} + (c_{AlN} - c_{GaN})x$, wherein c_{GaN} represents a c-axis length of GaN, and c_{AlN} represents a c-axis length of AlN; $M_x = M_{Ga} + (M_{Al} - M_{Ga})x$, wherein M_{Ga} represents the atomic weight of Ga, and M_{Al} represents the atomic weight of Al; M_N represents the atomic weight of nitrogen; and N_a represents Avogadro's number.

Major distinguishing features of the presently claimed invention are found in:

That is, distinguishing features of the claimed invention are found in (1) a nitride semiconductor substrate having a diameter of 10 mm or more comprising a nitride semiconductor layer having a basic composition represented by $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$), and (2) the mass density of the nitride semiconductor layer is 98% or more of a theoretical mass density p(x).

Nakayama actually discloses a nitride semiconductor wafer having a diameter larger than 45 mm; a single-mode **distortion** which has a maximum or a minimum of a central height H less than 12 μm (12,000 nm) or a distortion curvature radius R longer than 21 μm, a top surface roughness satisfying 0.1 nm ≤ RMS ≤ 5 nm; and a bottom surface roughness satisfying 0.1 nm ≤ RMS ≤ 5000 nm (claim 1 of Nakayama).

With respect to the method for producing the GaN single crystal substrate, Nakayama states in [0017], lines 3-9 that:

"50 mmϕ (2-inchϕ) freestanding GaN single crystal wafers are not produced on a commercial scale and do not come onto the market yet. The

applicant of the present invention has a potential of making a circular 50 mmϕ freestanding GaN single crystal wafer. 45 mmϕGaN wafers are also available for the applicant,"

However, a close examination of Nakayama shows the rather vague nature of the disclosure on production methods in Nakayama. Specifically, referring to [0098] of Nakayama, Nakayama discloses as follows:

> 2-inchϕ free standing wafers are made by an HVPE method which grows GaN films on a GaAs circular undersubstrate from a Ga-melt, HCl gas and NH_3 gas in a furnace by reactions of Ga+HCl→GaC1 and GaC1+NH_3→GaN. The HVPE method make the best use of the ELO (epitaxial lateral overgrowth) and the facet-growth which produces intentionally facet pits or gathering dislocation at bottoms of the pits and eliminates the GaAs undersubstrate and obtains a low-dislocation freestanding thick GaN film.

As can be seen from[0098], Nakayama provides substantially no details on the method adopted by Nakayama of forming what Nakayama calls "GaN free standing wafers... made by an HVPE method...".

Essentially Nakayama merely refers to an HVPE method without giving any details on the production conditions.

Given the above vagueness in Nakayama, one skilled in the art would not be able to ascertain or, in fact, reach any conclusion as to whether or not the Nakayama method provides a

GaN single crystal substrate comprising a nitride semiconductor layer whose mass density of the nitride semiconductor layer being 98% or more of a theoretical mass density ($\rho(x)$.

The claims of the present application, in distinction to Nakayama, recite a mass density of 98% or more of theoretical mass density defined using a very specific formula.

Nakayama is completely silent regarding any mass density parameter and this, of course, does not teach or suggest any mass density for the Nakayama nitride semiconductor layer.

Simply stated, Nakayama is directed to providing a gross-polishing method for reducing inherent distortion of nitride wafers (see [0028] from line 2 up, page 3 to line 1, page 4; and [0029] at page 4 of Nakayama.

In contrast to Nakayama, one major distinguishing feature of the present invention is found in distinguishing feature (2) above, i.e., the mass density of the nitride semiconductor layer is 98% or more of a theoretical mass density $\rho(x)$.

This distinguishing feature is not automatically satisfied by all GaN single crystal substrates. For instance, Example 1(a single-layer structure) and Example 2 (a multi-layer structure) in the specification of the present application specifically describe methods for producing the nitride semiconductor substrate comprising a nitride semiconductor layer according to an HVPE method, where the mass density of the nitride semiconductor layers is 98% or more of theoretical mass density $\rho(x)$ (see page 13 to page 15 of the specification). In distinction, in Comparative Example 1 (a single-layer structure) in the specification of the present application about 97% of a theoretical mass density $\rho(x)$ of the GaN single crystal substrate was obtained also using HVPE method (see page 15, lines 16-27 of the specification).

Quite clearly, GaN single crystal substrates can and will have various mass densities, which include mass densities falling outside the mass density of the nitride semiconductor defined in the present claims. The mass density of the nitride semiconductor substrate is dependent on the method for producing the nitride semiconductor substrate per se. As an integral part of the present invention, it is the **recognition and appreciation** of how to obtain the discussed mass density that enables the object of the present invention to be obtained, namely, to provide a high-quality nitride semiconductor substrate with a **reduced defect density**. Present specification, page 3, lines 20-23.

If the Examiner will refer to the present specification beginning at page 3, line 26 and continuing over to the top of page 4, intense research led the present inventors to find that the level of large-area defects in crystals such as impurities, nitrogen dissociation, polycrystals, voids, etc., can be avoided by increasing the mass density as an index to a desired level. It is this **recognition and appreciation** that mass density is a critical parameter that is lacking in the prior art.

Certainly if the Examiner has posed a prima facie case of obviousness, and Applicant submits this is not the case, any such case is rebutted by the data in the specification above discussed and the decisions later discussed. In short, Applicants respectfully submit that **based on this record** there is insufficient evidence presented by the Examiner to carry the burden to shift rebuttal to Applicant's on the issue of a 98% theoretical mass density being inherently disclosed in Nakayama.

As earlier stated, Nakayama is, of course, silent regarding a mass density of 98% or more of theoretical. A careful review of Nakayama shows that the Nakayama nitride wafers inherently have distortion based on inner stress. Nakayama, it appears, solves this problem by providing a gross-polishing method; see Nakayama [0028], [0030] and [0031].

For all of the above reasons, withdrawal of the rejection of claim 1 over Nakayama is requested.

Applicants rely on their arguments regarding claim 1 to support the withdrawal of the rejection of claims 2-7.

Applicant does with wish to separately address claim 15, which calls for the nitride semiconductor substrate according to claim 1 being grown by a hydride vapor-phase epitaxy method. Following this method, one is able to obtain a high-quality nitride semiconductor substrate with a mass density of, e.g., 5.920-6.090 g/cm^3, about 98-100% of a theoretical mass density $\rho(x)$, making it possible to produce devices from such substrate, such as LDs, et., having high reliability (see page 7, lines 12-18; and pages 13-14 of the specification).

Applicants submit that one skilled in the art, referring to Nakayama, which fails to teach or suggest any HVPE method in detail to provide a GaN single crystal substrate comprising a nitride semiconductor layer as well as the mass density of the nitride semiconductor layer of GaN with 98% or more of theoretical mass density $\rho(x)$, would not find claim 15 to be anticipated or be motivated to reach the invention of claim 15, and, accordingly, claim 15 of the present application is not anticipated or rendered obvious to Nakayama.

With respect to the patentability of claims 16-21, Applicants rely upon the arguments regarding claim 15.

Applicant further submits that as a matter of law, the Examiner's anticipation rejection is proper for the reason they have earlier advanced during prosecution.

It is well settled that to support an anticipation rejection based on grounds of inherency **some basis** must be advanced for the conclusion of inherency. What is lacking in the present Action is any basis to support the fact that claims 4, 5 and 7 represent mere inherent characteristics of Nakayama.

In this regard, *Ex parte* Skinner, 2 USPQ2d 1788 (Bd. Pat. App. & Int. 1986) is relevant.

Although dealing with claims directed to a mold of the type used to produce plastic articles, the Board had the following comments on an anticipation rejection where the Examiner found that the properties of the mold surface may be inherent characteristics of the reference coating.

> It is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office. *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984) quoting *In re Warner*, 379 F.2d 1011, 1016 154 USPQ 173, 177 (CCPA 1967). It is the Examiner's position that the mold of Mizutani may inherently have the characteristics of the claimed mold. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. *In re Oelrich*, 666 F.2d 578, 581, 212 USPQ 323 (CCPA 1981). We are mindful that there is a line of cases represented by *In re Swinehart*, 439 F.2d 210, 169 USPQ 226 (CCPA 1971) which indicates that where an Examiner has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, the Examiner possesses the authority to require an applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on. Nevertheless, before an applicant can be put to this burdensome task, the Examiner must provide some evidence or

> scientific reasoning to establish the reasonableness of the Examiner's belief that the functional limitation is an inherent characteristic of the prior art. In the case before us, no such evidence or reasoning has been set forward.

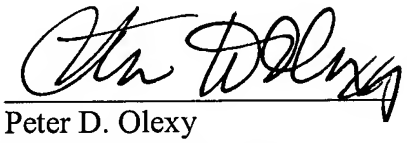
This similar effect is *Ex parte Schricker*, 56 USPQ2d 1723 (Bd. Pat. App. & Int. 2000), unpublished, which is relevant for the following discussion of the Board regarding inherency rejections:

> Inherency and obviousness are somewhat like oil and water - they do not mix well. Claimed subject matter can be anticipated because a prior art reference describes a method which inherently meets the limitations of a claimed method. Claimed subject matter can be unpatentable for obviousness when, notwithstanding a difference between that subject matter and a prior art reference, the claimed subject matter, as a whole, would have been obvious. **However, when an Examiner relies on inherency, it is incumbent on the Examiner to point to the "page and line" of the prior art which justifies an inherency theory.** Compare *In re Rijckaert*, 9 F.3d 1531, 1533, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (when the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the prior art) (citing *In re Yates*, 663 F.2d 1054, 1057, 211 USPQ 1149, 1151 (CCPA 1981)". (bolding added by the undersigned).

Applicants respectfully submit that in the present rejection, the Examiner has not carried his burden of proof, and respectfully request withdrawal of the rejection.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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